Remarks

Claims 1 -20 are pending in this application. Claims 3, 7, and 8 have been amended. The examiner has rejected claims 1-20 as being obvious under 35 U.S.C. § 103(a) over U.S. Patent No. 6,282,601 to Goodman et al, in view of U.S. Patent Application No. 20040019722 to Sedmak.

A. Independent Claims 1 and 15

The Examiner recognizes that Goodman does not teach or suggest all of the elements of the claimed invention. In particular, the Examiner recognizes that Goodman does not teach or suggest the following element of independent claims 1 and 15:

> wherein each of the processors is operable to enter an interrupt mode and wherein a uniquely addressable semaphore in memory is associated with each processor and indicates whether the associated processor has exited the interrupt mode.

(Office Action, p.2). The element provides that each of the processors can enter an interrupt mode, and memory includes a uniquely addressable semaphore for each processor that identifies when the associated processor has exited interrupt mode. The examiner points to Sedmak Figures 1 and 3 and paragraphs 0016 and 0026 as teaching this element. However, Sedmak fails to teach or suggest this element.

First, Figure 1 of Sedmak teaches a *single* processor with multiple cores. This can be seen by noting that there is only one label for "processor IC" (102) in the figure, which includes labels for a "core 1" (104(1)) and a "core 2" (104(2)). This does not teach or suggest multiple *processors*, as required by claims 1 and 15.

Second, Sedmak does not teach or suggest processors which are able to enter into an interrupt mode. Sedmak describes an arbitration method for obtaining access to a common

resource. (Sedmak, Abstract) Figure 3, step 308 and paragraphs 0025 and 0026 of Sedmak discuss setting a request bit in a register of a core to release a semaphore. This does not in any way teach or suggest processors entering (or exiting) an **interrupt mode**. A core holding or releasing a semaphore is not the same as a processor entering or exiting an interrupt mode. Sedmak is silent regarding interrupts and interrupt modes, and thus, Sedmak does not teach or suggest processors which are able to enter into an interrupt mode, as required by claims 1 and 15.

Third, Sedmak does not teach or suggest a uniquely addressable semaphore in memory, associated with each processor, which indicates whether the associated processor has exited the interrupt mode. The Examiner states that the semaphores are stored in control registers 106(1) and 106(2). (Office Action, p.3) However, Sedmak in Figure 1 teaches cores requesting (through *request and grant bits* in their registers) a *single* semaphore (not shown) which controls access to multiple resources, not multiple semaphores stored in the registers, as stated by the Examiner. (Sedmak, [0018]). Even when Sedmak discusses multiple semaphores, *only one* of the cores 104(1) or 104(2) may be granted a semaphore at a time. (Sedmak, [0019]). That is, a core is *not uniquely associated* with a semaphore; a core must always request and be *exclusively* granted a semaphore through the arbitration unit. (Sedmak, [0017]) Thus, Sedmak does not teach or suggest multiple semaphores, **each** of which is **associated** with one of the multiple processors in the computer system, such that each semaphore may be accessed **independently** and in a **non-exclusive** manner, as described by the Applicant's Specification (Spec., p.5:10-15) Additionally, Sedmak does not teach or suggest uniquely addressable semaphores stored in memory. The Examiner states that the semaphores are stored in the control registers 106. This is not the same as memory. Also, Sedmak specifically alludes to system memory semaphores as being *outside of the embodiments* of Sedmak's invention. (Sedmak,

[0008], [0009]) Additionally, the Examiner provides no evidence as to how Sedmak teaches or suggests uniquely addressable semaphores, or how Sedmak teaches or suggests that the semaphores are stored in a memory location which is offset from a base memory location by a unique offset indicator. (Office Action, p.3) Finally, as stated above, Sedmak does not teach or suggest interrupts or an interrupt mode, and thus Sedmak does not teach or suggest a semaphore which indicates when an associated processor has exited an interrupt mode.

For the reasons presented above, Sedmak does not cure the deficiencies of Goodman, and the combination fails to teach or suggest all of the elements of independent claims 1 and 15. Thus, a prima facie case of obviousness is not shown, and the rejection of independent claims 1 and 15 should be withdrawn.

B. Independent Claim 8

Like independent claims 1 and 15, independent claim 8 has been rejected on the basis of the combination of Goodman and Sedmak. For reasons similar to those presented above regarding independent claims 1 and 15, all of the elements of claim 8 are not taught or suggested by the combination of Goodman and Sedmak. Specifically, Sedmak does not teach or suggest setting a semaphore or negating a semaphore associated with a processor to *indicate that a processor has exited interrupt mode*. As stated above, the request bit and grant bit in the register of a core are not equivalent to a semaphore stored in memory. Additionally, these bits are directed to obtaining access via an arbiter to a shared resource. These bits do not in any way indicate that a processor has exited an interrupt mode. Finally, as stated above, step 308 of figure 3 in Sedmak is unrelated to a processor exiting an interrupt mode, rather, teaching only that a core has released hold of a semaphore.

Because the elements of claim 8 are not shown by the combination of Goodman and Sedmak, a prima facie case of obviousness is not shown and the rejection of claim 8 on obviousness grounds should be withdrawn.

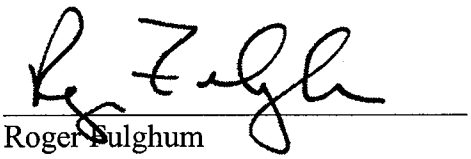
B. The Rejection of Dependent Claims 2-7, 9-14, and 16-20

The rejection of dependent claims 2-7, 9-14, and 16-20 will not be discussed individually herein, as each of these claims depends, either directly or indirectly, from an otherwise allowable base claim.

Conclusion

The applicant respectfully submits that the pending claims 1-20 of the present invention, as amended, are allowable. The applicant respectfully requests that the rejection of the pending claims be withdrawn and that these claims be passed to issuance.

Respectfully submitted,



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